

Subhajit Paul

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Research Interests

My research lies at the intersection of **Formal Verification** and **Artificial Intelligence**, where I work towards making hardware design and verification more reliable, explainable, and autonomous. I am particularly drawn to **agentifying verification workflows in Electronic Design Automation (EDA)** through Large Language Model (LLM) driven agents, and to studying coordinated decision-making via **Reinforcement Learning in Multi-Agent Environments**.

Education

The Neotia University <i>B.Tech. in Computer Science & Engineering</i> CGPA: 9/10	<i>Sep 2020 – Jun 2024</i>
Jhapardah Duke Institution <i>HS Education with PCM</i> Percentage: 82	<i>Jan 2018 – Feb 2020</i>

Experience

Indian Statistical Institute <i>Research Engineer</i> ○ Developed a novel framework to generate SystemVerilog Assertions using LLMs as a backbone to support reliable RTL development. ○ Researched the usefulness of LLMs in Model Reconciliation for robotic path planning. ○ Researching the application of the Agentic workflow in EDA for verification environment generation.	Kolkata, India <i>Jul 2024 – Present</i>
Xetalabs India <i>ML Engineer Intern</i> ○ Created an LLM-powered chat application for "Northeast Frontier Railway" to enable quick QA on their notice database. ○ Developed an OCR-to-vectorization pipeline for automated information retrieval from document images.	Guwahati, India <i>Jan 2024 – Jul 2024</i>

Publications

Formal Verification and Agentic AI.....	
LISA: LLM-Informed SystemVerilog Assertion Generation <i>Subhajit Paul, Ansuman Banerjee, Sumana Ghosh</i> Accepted at IEEE Computer Society Annual Symposium on VLSI (ISVLSI 2025).	Indian Statistical Institute, Kolkata <i>2025</i>
SuperSAGA: A Supervisor-Subordinate Agent for Assertion Generation <i>Subhajit Paul, Ansuman Banerjee, Sumana Ghosh</i> Accepted at 31st Asia and South Pacific Design Automation Conference (ASP-DAC Special Sessions 2026).	Indian Statistical Institute, Kolkata <i>2026</i>
VISTA: An Agentic Workflow for Formal Verification Environment Synthesis <i>Subhajit Paul, Ansuman Banerjee, Sumana Ghosh</i> Under Review and Submitted to the ACM Journal on Emerging Technologies in Computing Systems.	Indian Statistical Institute, Kolkata <i>2026</i>
LLMs in Robotics.....	
LLM-Guided Reconciliation for Explainable Robotic Path Planning <i>Subhajit Paul, Ansuman Banerjee</i> Accepted at IEEE Autonomic Computing and Self-Organizing Systems (ACSOS 2025).	Indian Statistical Institute, Kolkata <i>2025</i>

Ongoing Research Work

Multi-Agent Reinforcement Learning.....	
Exploring cooperative and competitive learning among autonomous agents, focusing on coordination, credit assignment, and emergent behaviour in complex multi-agent settings.	
LLM-based Agentic Systems.....	
Building tool-augmented, supervisor-subordinate LLM agents that plan, reason, and self-correct to automate formal verification and environment synthesis within EDA pipelines.	

Projects

LISA: LLM Informed SystemVerilog Assertion Generation

2024 – 2025

- A framework that uses LLMs and RAG to automatically generate, analyze, and iteratively refine SystemVerilog Assertions (SVAs).
- Tools: OpenAI API, Anthropic Claude API, Ollama, Cadence Jaspergold, ChromaDB
- Programming Languages: Python, SystemVerilog.
- **GitHub:** <https://github.com/Subhajit-Paul/LISA>

KG: Knowledge Graph Construction for Hardware Verification

2025

- Built a domain-specific Knowledge Graph (KG) pipeline that ingests hardware RTL and design specifications
- This framework can extract entities, relationships, and structural design context
- Tools: GraphRAG, pyverilog, OpenAI API.
- Programming Languages: Python.
- **GitHub:** <https://github.com/Subhajit-Paul/KG>